the rounded p-n junction interface closest to the trench wall surface is substantially co-planar with said corresponding trench wall surface and a channel width of a channel region for said JFET is approximately equal to a width of said source region between trench walls of said JFET; and

a gate surface reduction trench formed in said implanted gate region.

9. The JFET of claim **8** wherein said JFET is an n-channel JFET.

10. The JFET of claim **9** wherein said JFET is an enhancement mode JFET.

11. The JFET of claim **9** wherein said JFET is a depletion mode JFET.

12. The JFET of claim **8** wherein said JFET is a p-channel JFET.

13. The JFET of claim **12** wherein said JFET is an enhancement mode JFET.

14. The JFET of claim **12** wherein said JFET is a depletion mode JFET.

15. A transistor structure comprising:

a) a semiconducting substrate further comprising a drain region and a source region;

b) at least one gate region forming a p-n junction with a channel between said source region and said drain region;

c) a gate definition spacer adjacent to a corresponding trench wall surface, wherein said corresponding trench wall surface defines one side of a trench previously formed in a substrate wherein said corresponding trench wall surface forms a boundary between said gate definition spacer and a source region adjacent to said gate definition spacer, and wherein said at least one gate region comprises at least one rounded p-n junction interface formed at a corner of said implanted gate region due to annealing, wherein said at least one gate region extends laterally towards said channel such that at least a segment of the rounded p-n junction interface closest to the trench wall surface is substantially co-planar with said corresponding trench wall surface and a channel width for said channel is approximately equal to a width of said source region between trench walls of said transistor structure; and

d) a gate surface reduction trench formed in said implanted gate region.

16. The transistor structure of claim **15** wherein said semiconducting substrate is an n-type substrate.

17. The transistor structure of claim **16** wherein said structure includes two gate regions having merged depletion regions.

18. The transistor structure of claim **16** wherein said structure includes two gate regions, wherein each of said gate regions has an associated depletion region, and wherein said depletion regions are separated by a conductive channel.

19. The transistor structure of claim **15** wherein said semiconducting substrate is a p-type substrate.

20. The transistor structure of claim **19** wherein said structure includes two gate regions having merged depletion regions.

21. The transistor structure of claim **19** wherein said structure includes two gate regions, wherein each of said gate regions has an associated depletion region, and wherein said depletion regions are separated by a conductive channel.

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